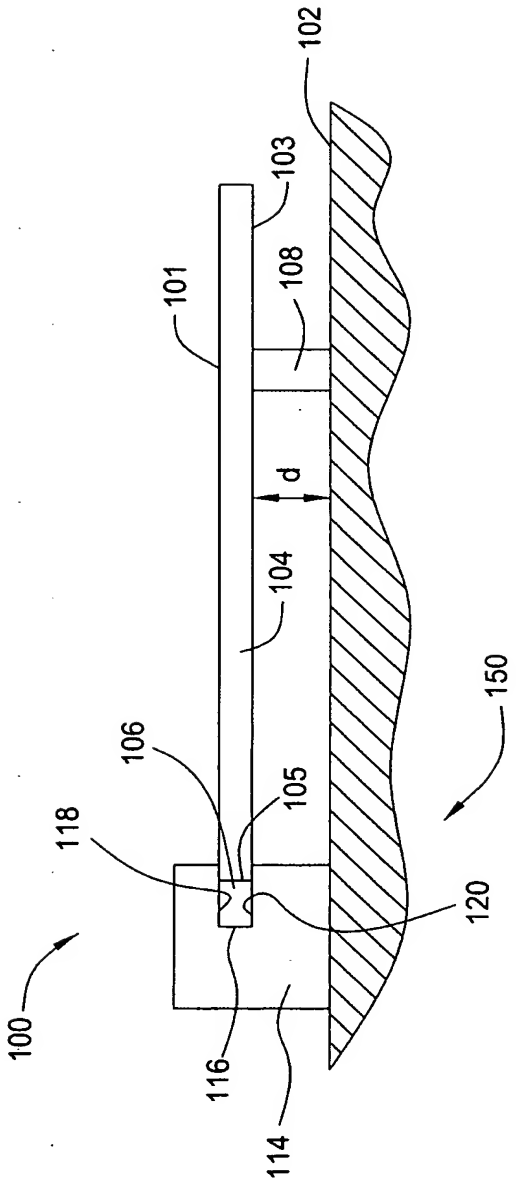


FIG. 1

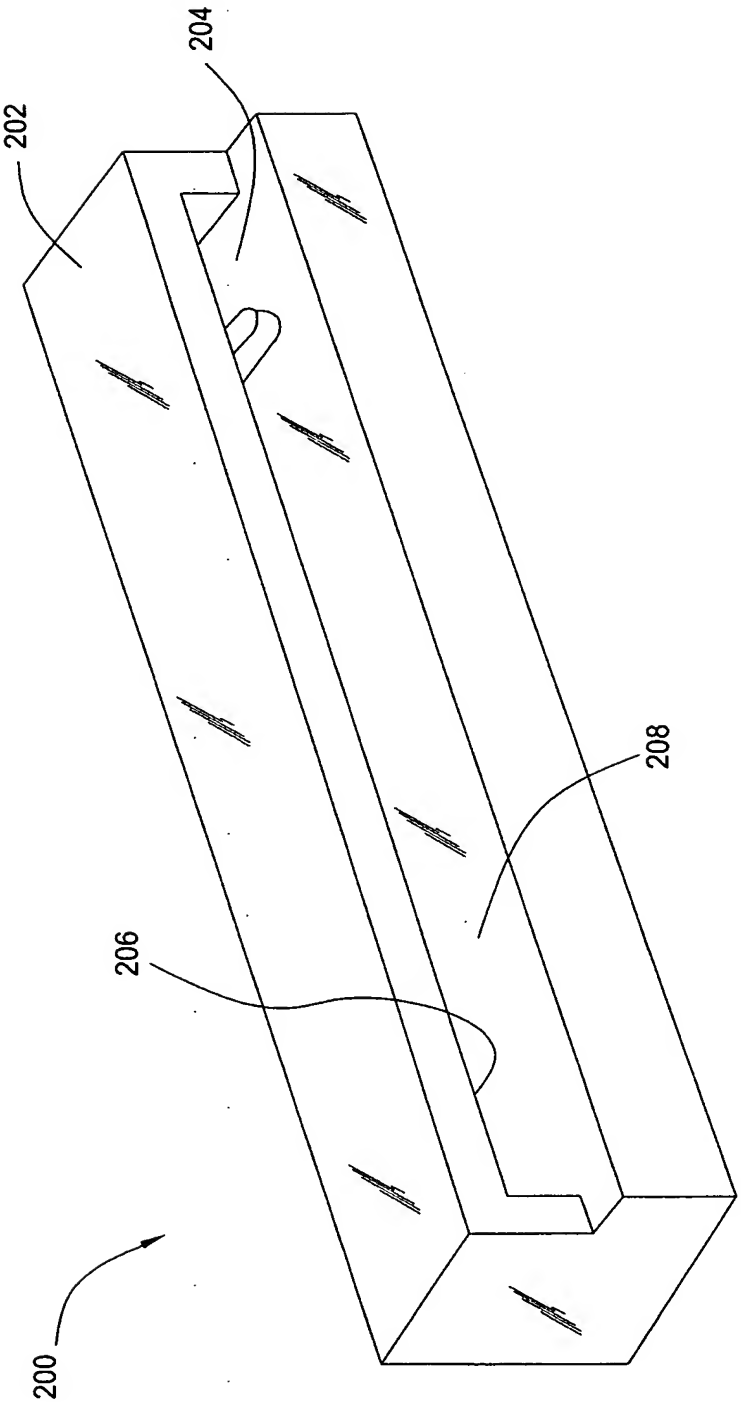


FIG. 2

| Pin# | Signal Name | Pin# | Signal Name |
|---|---|---|---|
| 1 | PWR_SRC | 2 | 5VRUN |
| 3 | PWR_SRC | 4 | RUNPWROK# |
| 5 | PWR_SRC | 6 | 1V8RUN |
| 7 | PWR_SRC | 8 | 1V8RUN |
| 9 | PWR_SRC | 10 | 1V8RUN |
| 11 | PWR_SRC | 12 | 1V8RUN |
| 13 | PWR_SRC | 14 | 1V8RUN |
| 15 | PWR_SRC | 16 | 1V8RUN |
| 17 | GND | 18 | 1V8RUN |
| 19 | GND | 20 | GND |
| 21 | GND | 22 | GND |
| 23 | GND | 24 | GND |
| 25 | KEY | 26 | KEY |
| 27 | KEY | 28 | KEY |
| 29 | KEY | 30 | KEY |
| 31 | KEY | 32 | KEY |
| 33 | KEY | 34 | KEY |
| 35 | KEY | 36 | KEY |
| 37 | PEX_RX15# | 38 | PRSNT2# |
| 39 | PEX_RX15 | 40 | PEX_TX15# |
| 41 | GND | 42 | PEX_TX15 |
| 43 | PEX_RX14# | 44 | GND |
| 45 | PEX_RX14 | 46 | PEX_TX14# |
| 47 | GND | 48 | PEX_TX14 |
| 49 | PEX_RX13# | 50 | GND |
| 51 | PEX_RX13 | 52 | PEX_TX13# |
| 53 | GND | 54 | PEX_TX13 |
| 55 | PEX_RX12# | 56 | GND |
| 57 | PEX_RX12 | 58 | PEX_TX12# |
| 59 | GND | 60 | PEX_TX12 |
| 61 | PEX_RX11# | 62 | GND |
| 63 | PEX_RX11 | 64 | PEX_TX11# |
| 65 | GND | 66 | PEX_TX11 |
| 67 | PEX_RX10# | 68 | GND |
| 69 | PEX_RX10 | 70 | PEX_TX10# |
| 71 | GND | 72 | PEX_TX10 |
| 73 | PEX_RX9# | 74 | GND |
| 75 | PEX_RX9 | 76 | PEX_TX9# |
| 77 | GND | 78 | PEX_TX9 |
| 79 | PEX_RX8# | 80 | GND |
| 81 | PEX_RX8 | 82 | PEX_TX8# |
| 83 | GND | 84 | PEX_TX8 |
| 85 | PEX_RX7# | 86 | GND |

| Pin# | Signal Name | Pin# | Signal Name |
|---|---|---|---|
| 87 | PEX_RX7 | 88 | PEX_TX7# |
| 89 | GND | 90 | PEX_TX7 |
| 91 | PEX_RX6# | 92 | GND |
| 93 | PEX_RX6 | 94 | PEX_TX6# |
| 95 | GND | 96 | PEX_TX6 |
| 97 | PEX_RX5# | 98 | GND |
| 99 | PEX_RX5 | 100 | PEX_TX5# |
| 101 | GND | 102 | PEX_TX5 |
| 103 | PEX_RX4# | 104 | GND |
| 105 | PEX_RX4 | 106 | PEX_TX4# |
| 107 | GND | 108 | PEX_TX4 |
| 109 | PEX_RX3# | 110 | GND |
| 111 | PEX_RX3 | 112 | PEX_TX3# |
| 113 | GND | 114 | PEX_TX3 |
| 115 | PEX_RX2# | 116 | GND |
| 117 | PEX_RX2 | 118 | PEX_TX2# |
| 119 | GND | 120 | PEX_TX2 |
| 121 | PEX_RX1# | 122 | GND |
| 123 | PEX_RX1 | 124 | PEX_TX1# |
| 125 | GND | 126 | PEX_TX1 |
| 127 | PEX_RX0# | 128 | GND |
| 129 | PEX_RX0 | 130 | PEX_TX0# |
| 131 | GND | 132 | PEX_TX0 |
| 133 | PEX_REFCLK# | 134 | PRSNT1# |
| 135 | PEX_REFCLK | 136 | TV_C |
| 137 | CLK_REQ# | 138 | GND |
| 139 | PEX_RST# | 140 | TV_Y |
| 141 | RSVD | 142 | GND |
| 143 | RSVD | 144 | TV_CVBS |
| 145 | SMB_DAT | 146 | GND |
| 147 | SMB_CLK | 148 | VGA_RED |
| 149 | THERM# | 150 | GND |
| 151 | VGA_HSYNC | 152 | VGA_GRN |
| 153 | VGA_VSYNC | 154 | GND |
| 155 | DDCA_CLK | 156 | VGA_BLU |
| 157 | DDCA_DAT | 158 | GND |
| 159 | IGP_UCLK# | 160 | LVDS_UCLK# |
| 161 | IGP_UCLK | 162 | LVDS_UCLK |
| 163 | GND | 164 | GND |
| 165 | IGP_UTX3# / RSVD | 166 | LVDS_UTX3# |
| 167 | IGP_UTX3 / RSVD | 168 | LVDS_UTX3 |
| 169 | RSVD | 170 | GND |

FIG. 3A

| Pin# | Signal Name | Pin# | Signal Name |
|---|---|---|---|
| 171 | IGP_UTX2# | 172 | LVDS_UTX2# |
| 173 | IGP_UTX2 | 174 | LVDS_UTX2 |
| 175 | GND | 176 | GND |
| 177 | IGP_UTX1# | 178 | LVDS_UTX1# |
| 179 | IGP_UTX1 | 180 | LVDS_UTX1 |
| 181 | GND | 182 | GND |
| 183 | IGP_UTX0# | 184 | LVDS_UTX0# |
| 185 | IGP_UTX0 | 186 | LVDS_UTX0 |
| 187 | GND | 188 | GND |
| 189 | IGP_LCLK# / DVI_B_CLK# | 190 | LVDS_LCLK# |
| 191 | IGP_LCLK / DVI_B_CLK | 192 | LVDS_LCLK |
| 193 | DVI_B_HPD / GND | 194 | GND |
| 195 | IGP_LTX3# / RSVD | 196 | LVDS_LTX3# |
| 197 | IGP_LTX3 / RSVD | 198 | LVDS_LTX3 |
| 199 | GND | 200 | GND |
| 201 | IGP_LTX2# / DVI_B_TX2# | 202 | LVDS_LTX2# |
| 203 | IGP_LTX2 / DVI_B_TX2 | 204 | LVDS_LTX2 |

| Pin# | Signal Name | Pin# | Signal Name |
|---|---|---|---|
| 205 | GND | 206 | GND |
| 207 | IGP_LTX1# / DVI_B_TX1# | 208 | LVDS_LTX1# |
| 209 | IGP_LTX1 / DVI_B_TX1 | 210 | LVDS_LTX1 |
| 211 | GND | 212 | GND |
| 213 | IGP_LTX0# / DVI_B_TX0# | 214 | LVDS_LTX0# |
| 215 | IGP_LTX0 / DVI_B_TX0 | 216 | LVDS_LTX0 |
| 217 | DVI_A_HPD | 218 | GND |
| 219 | DVI_A_CLK# | 220 | DDCC_DAT |
| 221 | DVI_A_CLK | 222 | DDCC_CLK |
| 223 | GND | 224 | LVDS_PPEN |
| 225 | DVI_A_TX2# | 226 | LVDS_BL_BRGHT |
| 227 | DVI_A_TX2 | 228 | LVDS_BLEN |
| 229 | GND | 230 | DDCB_DAT |
| 231 | DVI_A_TX1# | 232 | DDCB_CLK |
| 233 | DVI_A_TX1 | 234 | 2V5RUN |
| 235 | GND | 236 | GND |
| 237 | DVI_A_TX0# | 238 | 3V3RUN |
| 239 | DVI_A_TX0 | 240 | 3V3RUN |
| 241 | GND | 242 | 3V3RUN |

FIG. 3B

| Signal Name | Input/Output | Description |
|---|---|---|
| **DVI_A_TX0-2, DVI_A_TX0-2#** | Output, 100 Ohm Diff | TMDS output for either single link DVI or dual link DVI |
| **DVI_A_CLK, DVI_A_CLK#** | Output, 100 Ohm Diff | TMDS clock for either single link DVI or dual link DVI |
| **DVI_A_HPD** | Input | TMDS panel detect |
| **DVI_B_TX0-2, DVI_B_TX0-2#** | Output, 100 Ohm Diff | TMDS output for either single link DVI or dual link DVI, upper bits for dual-link: Note: these pins are shared with IGP LVDS loop through pins |
| **DVI_B_CLK, DVI_B_CLK#** | Output, 100 Ohm Diff | TMDS clock, only used for second single-link DVI. Note: these pins are shared with IGP LVDS loop through pins |
| **DVI_B_HPD** | Input/GND | TMDS panel detect, only used for second single-link DVI. Tie to GND on motherboard if notebook is configured for IGP LVDS pass through |
| **DDCA_CLK** | Output, 3.3 V logic levels | Serial link, can connect to VGA, DVI-A or DVI-B. Configuration needs to be stored in MXM system information ROM |
| **DDCA_DAT** | BI-Directional | Serial link, can connect to VGA, DVI-A or DVI-B. Configuration needs to be stored in MXM system information ROM |
| **DDCB_CLK** | Output, 3.3 V logic levels | Serial link, can connect to VGA, DVI-A or DVI-B. Configuration needs to be stored in MXM system information ROM |
| **DDCB_DAT** | BI-Directional | Serial link, can connect to VGA, DVI-A or DVI-B. Configuration needs to be stored in MXM system information ROM |
| **LVDS_PPEN** | Output, 3.3 V logic levels | LVDS Panel Power enable |
| **LVDS_BLEN** | Output, 3.3 V logic levels | LVDS Panel backlight enable |
| **LVDS_BL_BRGHT** | PWM Output | LVSD Panel brightness control, duty cycle determines output level |
| **LVDS_UTX0-3, LVDS_UTX0-3#** | Output, 100 Ohm Diff | LVDS output for dual link |
| **IGP_UTX0-2, IGP_UTX0-2#** | Input, 100 Ohm Diff | LVDS input that loops back to **LVDS_UTX0-2, LVDS_UTX0-2#** to provide path for LVDS with IGP only. Note: these pins are shared with DVI_B pins |
| **LVDS_UCLK, LVDS_UCLK#** | Output, 100 Ohm Diff | LVDS clock for dual link |

FIG. 4A

| Signal Name | Input/Output | Description |
|---|---|---|
| **IGP_UCLK, IGP_UCLK#** | Input, 100 Ohm Diff | LVDS input that loops back to **LVDS_UCLK, LVDS_UCLK#** to provide path for LVDS with IGP only. Note: these pins are shared with DVI_B pins |
| **LVDS_LTX0-3, LVDS_LTX0-3#** | Output, 100 Ohm Diff | LVDS output for either single link or dual link |
| **IGP_LTX0-2, IGP_LTX0-2#** | Input, 100 Ohm Diff | LVDS input that loops back to **LVDS_LTX0-2, LVDS_LTX0-2#** to provide path for LVDS with IGP only. Note: these pins are shared with **DVI_B** pins |
| **LVDS_LCLK, LVDS_LCLK#** | Output, 100 Ohm Diff | LVDS clock for either single link or dual link |
| **IGP_LCLK, IGP_LCLK#** | Input, 100 Ohm Diff | LVDS input that loops back to **LVDS_LCLK, LVDS_LCLK#** to provide path for LVDS with IGP only. Note: these pins are shared with DVI_B pins |
| **TV_Y** | Output, 37.5 Ohm +/- 2 Ohms | **TV_OUT** Chroma |
| **TV_C** | Output, 37.5 Ohm +/- 2 Ohms | **TV_OUT** Luma |
| **TV_CVBS** | Output, 37.5 Ohm +/- 2 Ohms | **TV_OUT** Composite |
| **DDCC_CLK** | Output, 3.3 V logic levels | Serial link, connect to EDID LVDS Panel and to MXM System Information ROM. This link is not to be used for external interfaces |
| **DDCC_DAT** | BI-Directional | Serial link, connect to EDID LVDS Panel and to MXM System Information Rom. This link is not to be used for external interfaces |
| **VGA_BLU** | Output. 37.5 Ohm +/- 2 Ohms | **RGB** Output |
| **VGA_RED** | Output, 37.5 Ohm +/- 2 Ohms | **RGB** Output |
| **VGA_GRN** | Output, 37.5 Ohm +/- 2 Ohms | **RGB** Output |
| **VGA_HSYNC** | Output, 75 Ohm, 3.3 V logic levels | **RGB** Horizontal Sync |
| **VGA_VSYNC** | Output, 75 Ohm, 3.3 V logic levels | **RGB** Vertical Sync |
| **SMB_CLK** | Input, 5 V tolerant | Serial link for thermal sensor on GPU. Connect to motherboard's SMBus Clock signal. |
| **SMB_DAT** | Bi-Dir, 5 V tolerant | Serial link for thermal sensor on GPU. Connect to motherboard's SMBus Data signal. |
| **THERM#** | Output, active low | Indicates a thermal alert. Connect to motherboard's SMBus Alert signal. |
| **PRSNT1#** | GND | Card present detect, indicates if MXM module is present. Tie to pull-up on motherboard. If high then MXM is not present. If low then MXM is present. Can be used to control IGP upgrade multiplexers |

FIG. 4B

| Signal Name | Input/Output | Description |
|---|---|---|
| PRSNT2# | GND | Tied to Ground on both motherboard and MXM. Reserved for future functionality. |
| CLK_REQ# | Output, active low | Indicates need for PEX_REFCLK |
| PEX_RST# | Input, active low | PCI_Express reset |
| PEX_REFCLK, PEX_REFCLK# | Input, 100 Ohm Diff | PCI-Express reference clock. |
| PEX_TX0-15, PEX_TX0-15# | Input, 100 Ohm Diff | PCI-Express 16 lanes, output from northbridge |
| PEX_RX0-15, PEX_RX0-15# | Output, 100 Ohm Diff | PCI-Express 16 lanes, input to northbridge |
| RUNPWROK | Input | Indicates that all power to the MXM is within the specified tolerances |
| 3V3RUN | Power input | 3.3 V run power |
| 5VRUN | Power input | 5 V run power |
| 2V5RUN | Power input | 2.5 V run power |
| 1V8RUN | Power input | 1.8 V run power |
| PWR_SRC | Power input | Battery power |

FIG. 4C

| Voltage Rail | Voltage | Current | Power | Notes |
|---|---|---|---|---|
| 3V3RUN | 3.3 V +/- 5% | 1.5 Amps | 4.95 W | 3.3 V run |
| 5VRUN | 5 V +/- 5% | 0.5 Amps | 2.5 W | 5 V run |
| 2V5RUN | 2.5 V +/- 5% | 0.5 Amps | 1.25 W | 2.5 V run |
| 1V8RUN | 1.8 V +/- 5% | 3.5 Amps | 6.3 W | 1.8 V run |
| PWR_SRC | 7.5 V to 22 V | Up to 4 Amps | 8.9 W to 38.9 W | Battery, store power capability in MXM system information ROM |

FIG. 5

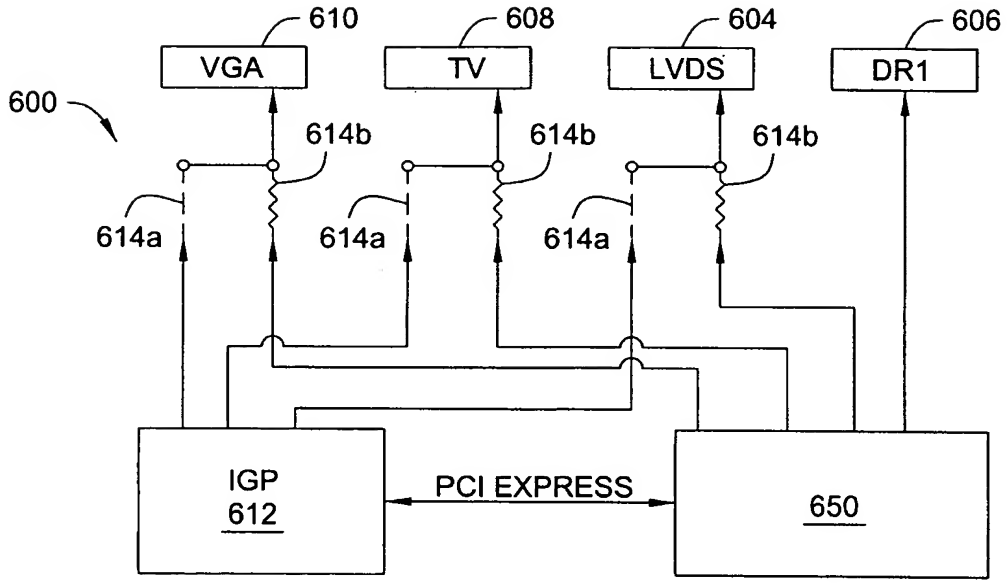
610
608
604
606
VGA
TV
LVDS
DR1
600
614b
614b
614b
614a
614a
614a
IGP
612
PCI EXPRESS
650

FIG. 6A

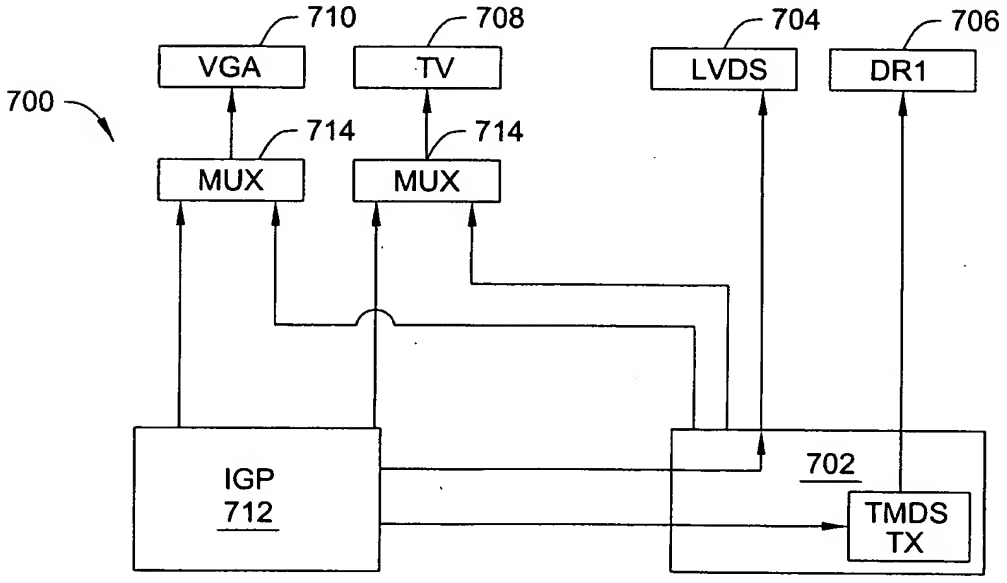
710
708
704
706
VGA
TV
LVDS
DR1
700
714
714
MUX
MUX
IGP
712
702
TMDS
TX

FIG. 7A

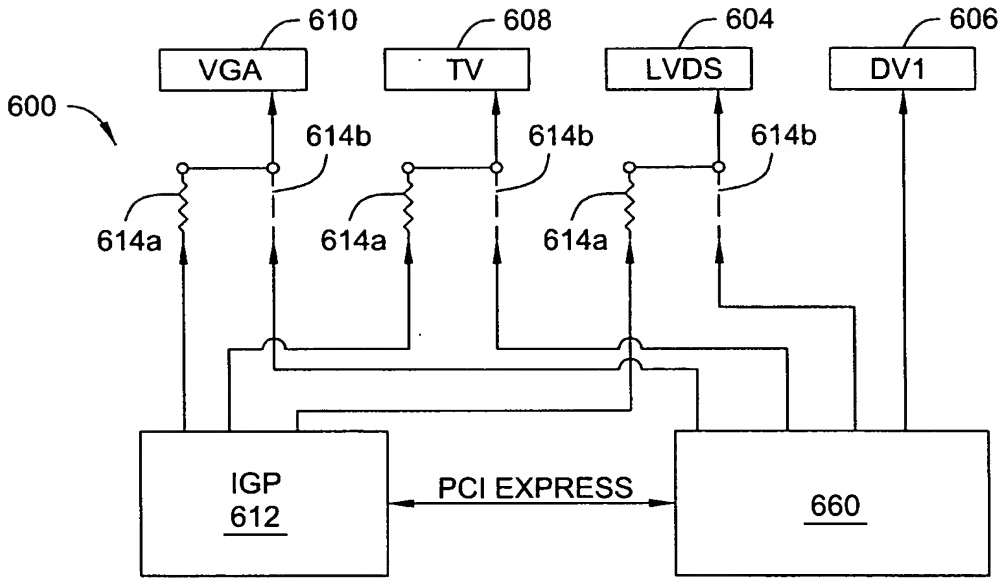
610
608
604
606
VGA
TV
LVDS
DV1
600
614b
614b
614b
614a
614a
614a
IGP
612
PCI EXPRESS
660

FIG. 6B

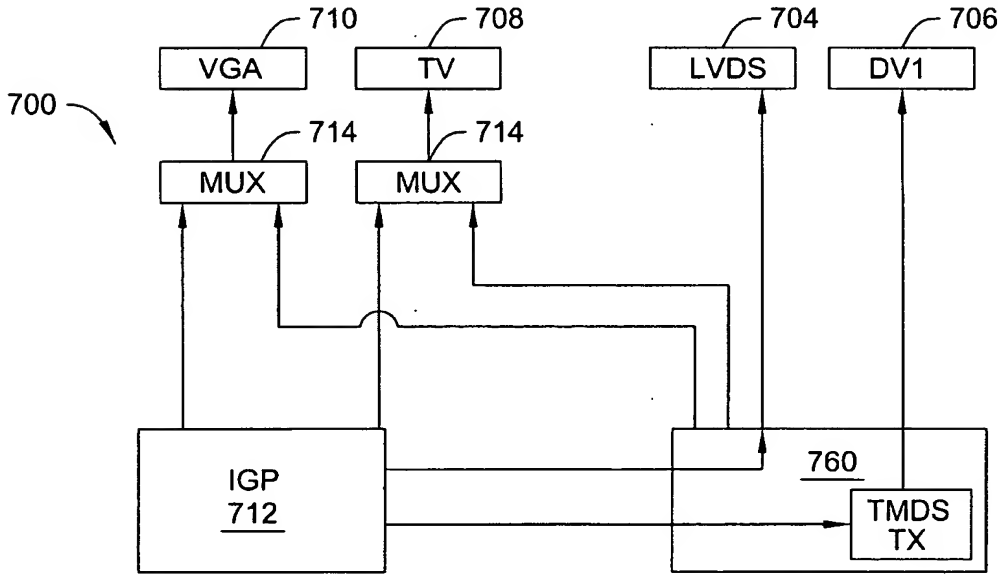
710
708
704
706
VGA
TV
LVDS
DV1
700
714
714
MUX
MUX
IGP
712
760
TMDS
TX

FIG. 7B